

10/549900
JC17 Rec'd PCT/PTO 20 SEP 2005



AMENDMENT

(Amendment based upon the provision of Article 11 of said Law)

To: Examiner of the Patent Office

1. Identification of the International Application

PCT/JP2004/004072

2. Applicant

Name: CANON KABUSHIKI KAISHA

Address: 3-30-2, Shimomaruko, Ohta-ku, Tokyo
146-8501 Japan

Country of Nationality: JAPAN

Country of Residence: JAPAN

3. Agent

Name: TAKANASHI, Norimichi



Address: No. 602, Fuji Bldg., 2-3, Marunouchi 3-chome,
Chiyoda-ku, Tokyo 100-0005 Japan

4. Item to be amended: Claims

5. Subject Matter of Amendment

The applicant has amended claim 1, and claims 2 to 4 are unchanged. The whole wording of claim 1 has been rewritten in order to make the feature of claim 1 clear. Support for change to "a non-doped layer stacked on the silicon substrate, the non-doped layer having an amorphous silicon phase and a microcrystalline silicon phase mixed together" can be found at page 9, line 25 to page 10, line 1 of the specification.

6. List of Attached Documents

(1) Replacement sheet of page 49

CLAIMS

1. (Amended) A solar cell comprising:
a silicon substrate for a solar cell, the
substrate comprising a base composed of a
5 polycrystalline metal-grade silicon solidified in one
direction and a high-purity polycrystalline silicon
layer stacked on a surface of the base; and
a non-doped layer stacked on the silicon
substrate, the non-doped layer having an amorphous
10 silicon phase and a microcrystalline silicon phase
mixed together.
2. (Unchanged) A solar cell according to claim
1, wherein a thickness of the layer having the non-
doped amorphous silicon phase and the
15 microcrystalline silicon phase mixed together ranges
from 1 nm to 15 nm.
3. (Unchanged) A solar cell according to claim
1 or 2, wherein a ratio of the amorphous silicon
phase and the microcrystalline silicon phase in the
20 layer having the non-doped amorphous silicon phase
and the microcrystalline silicon phase mixed together
ranges from 1:1 to 10:1.
4. (Unchanged) A solar cell comprising a
crystalline silicon substrate or a crystalline
25 silicon layer, a layer having an amorphous silicon
phase and a microcrystalline silicon phase mixed
together, and a polycrystalline silicon layer grown
with the microcrystalline silicon phase as a seed,
which are stacked in mentioned order.